IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

1. (Currently Amended) A device comprising:

a gate dielectric formed on first conductivity region of a substrate having recesses, wherein said recesses have an inwardly concaved geometry with inflection points;

a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a pair of silicon or silicon alloy inwardly concaved source/drain regions of a second conductivity type having a concentration of impurities in a range of $1x10^{18}/cm^3$ to $3x10^{21}/cm^3$ formed in said recesses in said substrate and on opposite sides of said gate electrode creating metallurgical inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer, wherein said silicon or silicon alloy source/drain regions extend the greatest distance laterally beneath said lower portion of the gate electrode at said inflection points, which occurs between 50-250Å laterally beneath said gate electrode and at a depth of between 25-100Å beneath said gate dielectric, and directly define a first channel region having a first metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and a second channel region having a second metallurgical length between said metallurgical inflection points, wherein said first metallurgical channel length directly beneath said lower

portion of said gate electrode is larger than said second metallurgical channel length between said metallurgical inflection points.

2. (Previously presented) The device of claim 1 wherein said silicon or silicon alloy source/drain regions extend above said gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric.

3. (Previously presented) The device of claim 1 wherein said gate dielectric layer is thicker beneath outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode.

4. (Previously presented) The device of claim 2 wherein said gate dielectric layer is thicker beneath said sidewall spacer and said outside edge of said gate electrode then the gate dielectric layer beneath the center of said gate electrode.

5. (Previously presented) The device of claim 1 further comprising a pair of silicon or silicon alloy regions having a first conductivity type region formed between said pair of silicon or silicon alloy source/drain regions of said second conductivity type and said first conductivity type region.

6. (Previously presented) The device of claim 5 wherein the concentration of said silicon or silicon alloy regions having a first conductivity type is greater than the concentration of said first conductivity type region.

7. (Canceled)

8. (Previously presented) The device of claim 1 wherein said first conductivity type is n-type conductivity and wherein said second conductivity type is p-type conductivity.

9. (Previously presented) The device of claim 1 wherein said first conductivity type is p-type conductivity and wherein said second conductivity type is n-type conductivity.

10. (Canceled)

11. (Currently Amended) The device of claim [[10]] 1 wherein the concentration of said silicon or silicon alloy source/drain regions of a second conductivity type is approximately $1x10^{21}/cm^3$.

12. (Previously presented) The device of claim 1 further comprising silicide formed on said silicon or silicon alloy source/drain regions.

13. (Currently Amended) A device comprising:

a gate dielectric formed on a first conductivity type region of a substrate having recesses, wherein the recesses have an inwardly concaved geometry with inflection points;

a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a pair of silicon-germanium alloy source/drain regions having a concentration of impurities of second conductivity type in a range of $1x10^{18}/cm^3$ to $3x10^{21}/cm^3$ formed in said recesses in said substrate and along opposite sides of said gate electrode wherein said silicon-germanium alloy source/drain regions in said recesses in said substrate are inwardly concaved and create metallurgical inflection points in said substrate directly beneath said lower portion of said gate electrode formed directly on said gate dielectric, wherein said silicon-germanium alloy source/drain regions extend the greatest distance laterally beneath said gate electrode at said inflection points which occurs between 50-250Å laterally beneath said gate electrode and at a depth of between 25-100Å beneath said gate dielectric, said silicon germanium alloy extends above the height of said gate dielectric layer wherein the top surface of said deposited silicon-germanium alloy is spaced further from said gate electrode than said silicon-germanium alloy adjacent to said gate dielectric.

14. (Previously presented) The device of claim 13 wherein said gate dielectric layer is thicker beneath said outside edges of said gate electrode then the gate dielectric beneath the center of the gate electrode.

15. (Currently Amended) A device comprising:

a gate dielectric formed on a first conductivity type region of a substrate having recesses, wherein the recesses have an inwardly concaved geometry with inflection points;

a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a pair of silicon-germanium alloy inwardly concaved source/drain regions of a second conductivity type having a concentration of impurities in a range of $1x10^{18}/cm^3 - 3x10^{21}/cm^3$ formed in said recesses in said substrate at opposite sides of said gate electrode creating metallurgical inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer and defining a first channel region having a first metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and a second channel region having a second metallurgical length between said metallurgical inflection points, wherein said first metallurgical channel length directly beneath said lower portion of said gate electrode is larger than said second metallurgical channel length between said metallurgical inflection points.